## FEATURES

- Guaranteed AC performance over temperature and voltage:
  - DC to > 10.7Gbps data throughput
  - DC to > 7GHz $f_{MAX}$ (clock)
  - < 240ps propagation delay
  - < 60ps $t_r$ / $t_f$ times
- Ultra-low crosstalk-induced jitter: < 0.7ps$_{rms}$
- Ultra-low jitter design:
  - < 1ps$_{RMS}$ random jitter
  - < 10ps$_{PP}$ deterministic jitter
  - < 10ps$_{PP}$ total jitter (clock)
- Unique input termination and $V_T$ pin accepts DC-coupled and AC-coupled inputs (CML, PECL, LVDS)
- Internal 50Ω output source termination
- Typical 400mV CML output swing ($R_L$ = 50Ω)
- Power supply 2.5V ±5% or 3.3V ±10%
- –40°C to +85°C temperature range
- Available in 16-pin (3mm × 3mm) MLF® package

## APPLICATIONS

- Redundant clock distribution
- OC-3 to OC-192 SONET/SDH clock/data distribution
- Loopback
- Fibre Channel distribution

Precision Edge®

## DESCRIPTION

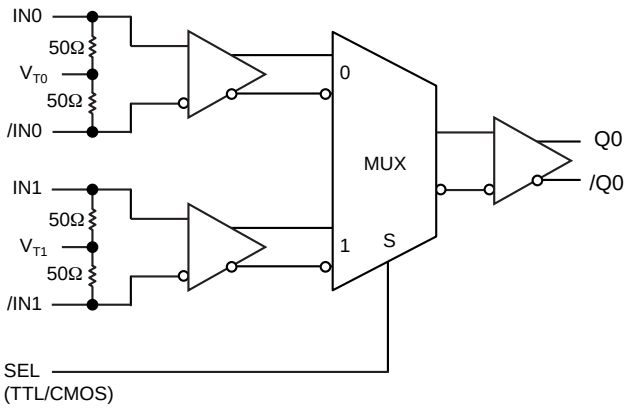
The SY58017U is a 2.5V/3.3V precision, high-speed, 2:1 differential MUX capable of handling clocks up to 7GHz and data up to 10.7Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows customers to interface to any differential signal (AC- or DC-coupled) as small as 100mV without any level shifting or termination resistor networks in the signal path. The outputs are 50Ω source terminated CML, with extremely fast rise/fall times guaranteed to be less than 60ps.

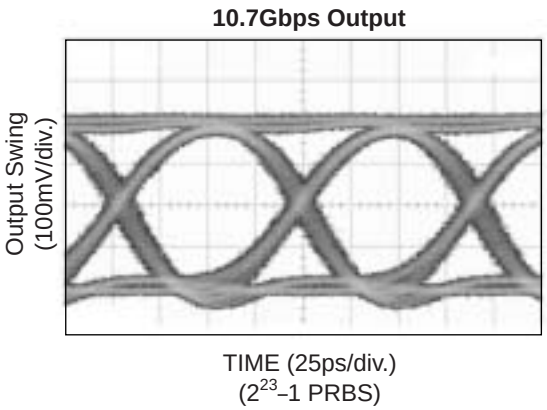
The SY58017U operates from a 2.5V ±5% supply or a 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. For applications that require LVPECL outputs, consider the SY58018U or SY58019U Multiplexers with LVPECL outputs. The SY58017U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at www.micrel.com.

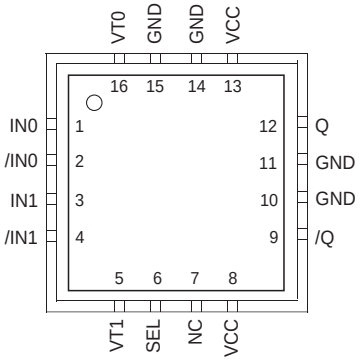
## FUNCTIONAL BLOCK DIAGRAM




## TYPICAL PERFORMANCE



## PACKAGE/ORDERING INFORMATION




**16-Pin MLF® (MLF-16)**

### Ordering Information(1)

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|---|---|---|---|---|
| SY58017UMI | MLF-16 | Industrial | 017U | Sn-Pb |
| SY58017UMITR(2) | MLF-16 | Industrial | 017U | Sn-Pb |
| SY58017UMG(3) | MLF-16 | Industrial | 017U with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY58017UMGTR(2, 3) | MLF-16 | Industrial | 017U with Pb-Free bar-line indicator | Pb-Free NiPdAu |

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at $T_A$ = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

## PIN DESCRIPTION

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1, 2<br>3, 4 | IN0, /IN0<br>IN1, /IN1 | Differential Input: These input pairs are the differential signal inputs to the device. They accept differential AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a $V_T$ pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the *"Input Interface Applications"* section for more details. |
| 16, 5 | VT0, VT1 | Input Termination Center-Tap: Each side of the differential input pair terminates to a $V_T$ pin. The $V_{T0}$ and $V_{T1}$ pins provide a center-tap to a termination network for maximum interface flexibility. See *"Input Interface Applications"* section for more details. |
| 6 | SEL | This single-ended TTL/CMOS compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. |
| 7 | NC | No connect. |
| 8, 13 | VCC | Positive Power Supply: Bypass with 0.1μF\|\|0.01μF low ESR capacitors. 0.01μF capacitor should be as close to $V_{CC}$ pin as possible. |
| 12, 9 | Q, /Q | Differential Outputs: This CML output pair is the output of the device. Normally terminate with 100Ω across Q and /Q. See *"Output Interface Applications"* section. It is a logic function of the IN0, IN1, and SEL inputs. Please refer to the *"Truth Table"* for details. |
| 10, 11, 14, 15 | GND, Exposed Pad | Ground. Ground pins and exposed pad must be connected to the same ground plane. |

## TRUTH TABLE

| SEL | Output |
|---|---|
| 0 | IN0 Input Selected |
| 1 | IN1 Input Selected |

## Absolute Maximum Ratings(1)

Power Supply Voltage ($V_{CC}$) ..... –0.5V to +4.0V
Input Voltage ($V_{IN}$) ..... –0.5V to $V_{CC}$
CML Output Voltage ($V_{OUT}$) ..... $V_{CC}$ –1.0V to $V_{CC}$ +0.5V
Termination Current(3)
Source or sink current on $V_T$ pin ..... ±100mA
Input Current
Source or sink current on IN, /IN pin ..... ±50mA
Lead Temperature (soldering, 20 sec.) ..... 260°C
Storage Temperature Range ($T_S$) ..... –65°C to +150°C

## Operating Ratings(2)

Power Supply Voltage ($V_{CC}$) ..... +2.375V to +2.625V
..... +3.0V to +3.6V
Ambient Temperature Range ($T_A$) ..... –40°C to +85°C
Package Thermal Resistance(4)
MLF® ($\theta_{JA}$)
Still-Air ..... 60°C/W
MLF® ($\psi_{JB}$)
Junction-to-Board ..... 38°C/W

## DC ELECTRICAL CHARACTERISTICS(5)

$T_A$ = –40°C to 85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | $V_{CC}$ = 2.5V<br>$V_{CC}$ = 3.3V | 2.375<br>3.0 | 2.5<br>3.3 | 2.625<br>3.6 | V<br>V |
| $I_{CC}$ | Power Supply Current | No load, max. $V_{CC}$(6) | | 55 | 70 | mA |
| $R_{DIFF\_IN}$ | Differential Input Resistance (IN0-to-/IN0, IN1-to-/IN1) | | 80 | 100 | 120 | Ω |
| $R_{IN}$ | Input Resistance (IN0-to-$V_{T0}$, /IN0-to-$V_{T0}$, IN1-to-$V_{T1}$, /IN1-to-$V_{T1}$) | | 40 | 50 | 60 | Ω |
| $V_{IH}$ | Input HIGH Voltage (IN0, /IN0, IN1, /IN1) | **Note 7** | $V_{CC}$–1.6 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage (IN0, /IN0, IN1, /IN1) | | 0 | | $V_{IH}$–0.1 | V |
| $V_{IN}$ | Input Voltage Swing (IN0, /IN0, IN1, /IN1) | See Figure 1a | 0.1 | | 1.7 | V |
| $V_{DIFF\_IN}$ | Differential Input Voltage Swing \|IN0, /IN0\|, \|IN1, /IN1\| | See Figure 1b | 0.2 | | | V |
| $V_{T\ IN}$ | IN to $V_T$ (IN0, /IN0, IN1, /IN1) | | | | 1.28 | V |

**Notes:**

1. Permanent device damage may occur if *"Absolute Maximum Ratings"* are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to *"Absolute Maximum Ratings"* conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. $\psi_{JB}$ uses 4-layer $\theta_{JA}$ in still-air measurment, unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. Includes current through internal 50Ω pull-ups.
7. $V_{IH}$ (min) not lower than 1.2V.

## CML OUTPUT DC ELECTRICAL CHARACTERISTICS[8]

$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $T_A$= –40°C to 85°C; $R_L$ = 100Ω across each output pair, or equivalent, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | | $V_{CC}$–0.020 | | $V_{CC}$ | V |
| $V_{OUT}$ | Output Voltage Swing | See Figure 1a | 325 | 400 | | mV |
| $V_{DIFF\_OUT}$ | Differential Output Voltage Swing | See Figure 1b | 650 | 800 | | mV |
| $R_{OUT}$ | Output Source Impedance | | 40 | 50 | 60 | Ω |

## LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS[8]

$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $T_A$= -40°C to 85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V |
| $I_{IH}$ | Input HIGH Current | | | | 40 | µA |
| $I_{IL}$ | Input LOW Current | | –300 | | | µA |

**Note:**

8. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## AC ELECTRICAL CHARACTERISTICS[9]

$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $T_A$= –40°C to 85°C, $R_L$= 100Ω across each output pair, or equivalent, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Operating Frequency | NRZ Data | 10.7 | | | Gbps |
| | | $V_{OUT}$ ≥ 200mV Clock | | 7 | | GHz |
| $t_{pd}$ | Differential Propagation Delay | IN-to-Q | 90 | 160 | 240 | ps |
| | | SEL-to-Q | 50 | 180 | 350 | ps |
| $t_{pd}$ Tempco | Differential Propagation Delay Temperature Coefficient | | | 75 | | fs/°C |
| $t_{SKEW}$ | Input-to-Input Skew | **Note 10** | | 4 | 15 | ps |
| | Part-to-Part Skew | **Note 11** | | | 100 | ps |
| $t_{JITTER}$ | Data Random Jitter | **Note 12** | | | 1 | $ps_{rms}$ |
| | Deterministic Jitter | **Note 13** | | | 10 | $ps_{p-p}$ |
| | Clock Cycle-to-Cycle Jitter | **Note 14** | | | 1 | $ps_{rms}$ |
| | Total Jitter | **Note 15** | | | 10 | $ps_{p-p}$ |
| | Crosstalk-Induced Jitter | **Note 16** | | | 0.7 | $ps_{rms}$ |
| $t_r$, $t_f$ | Output Rise/Fall Time | 20% to 80%, at full swing | 20 | 40 | 60 | ps |

**Notes:**

9. High-frequency AC parameters are guaranteed by design and characterization.
10. Input-to-input skew is the difference in time from and input-to-output in comparison to any other input-to-output. In addition, the input-input skew does not include the output skew.
11. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
12. RJ is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps/3.2Gbps.
13. DJ is measured at 2.5Gbps/3.2Gbps, with both K28.5 and $2^{23}$–1 PRBS pattern.
14. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n$–$T_{n-1}$ where T is the time between rising edges of the output signal.
15. Total jitter definition: with an ideal clock input of frequency ≤ $f_{MAX}$, no more than one output edge in $10^{12}$ output edges will deviate by more than the specified peak-to-peak jitter value.
16. Crosstalk is measured at the output while applying two similar frequencies that are asynchronous with respect to each other at the inputs.

## SINGLE-ENDED AND DIFFERENTIAL SWINGS

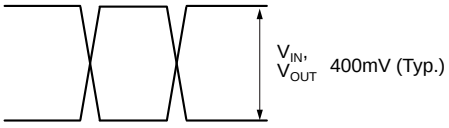



**Figure 1a. Single-Ended Voltage Swing**

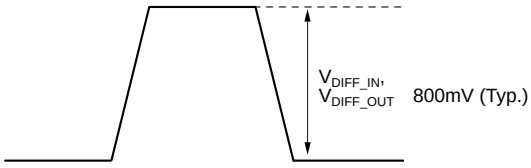
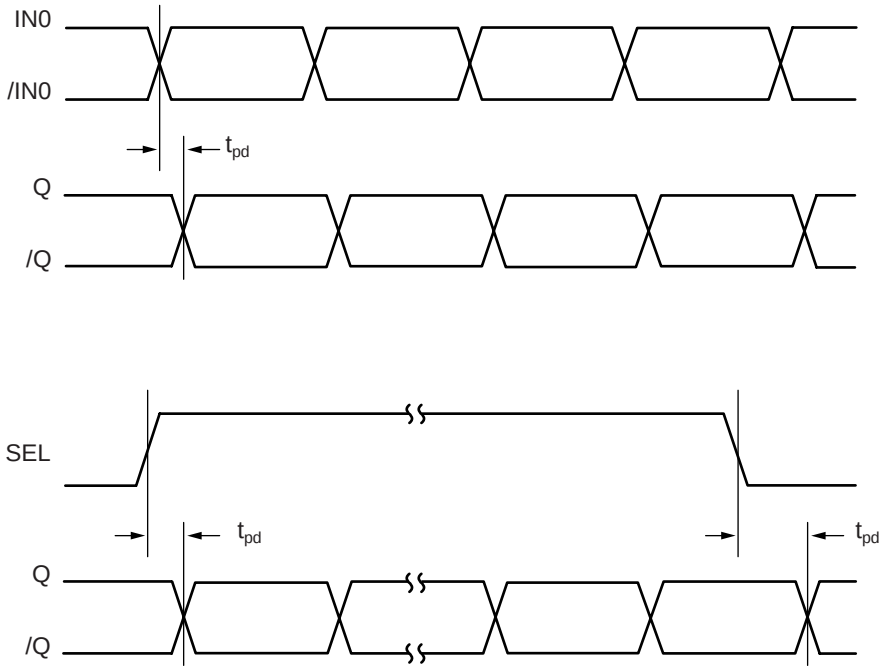



**Figure 1b. Differential Voltage Swing**

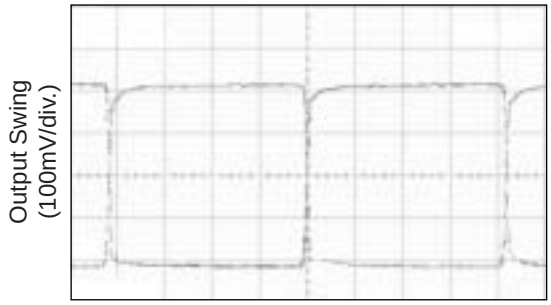
## TIMING DIAGRAMS



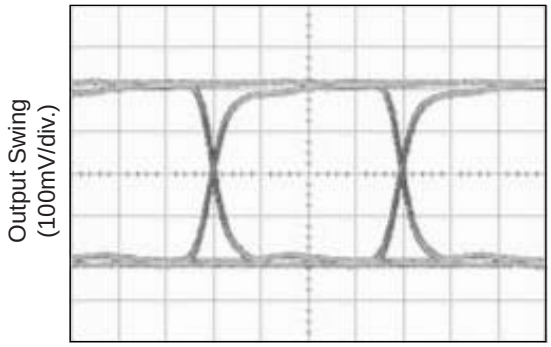
## TYPICAL OPERATING CHARACTERISTICS

$V_{CC}$ = 2.5V, $V_{IN}$ = 100mV, $T_A$ = 25°C, unless otherwise stated.

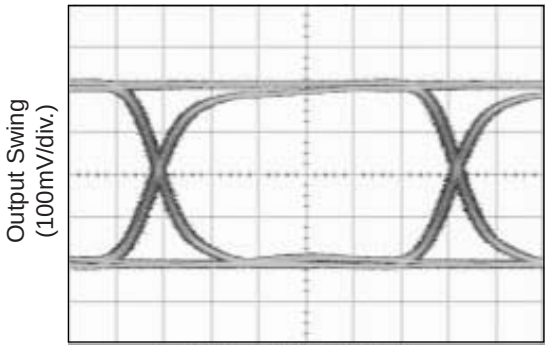
**200MHz Output**



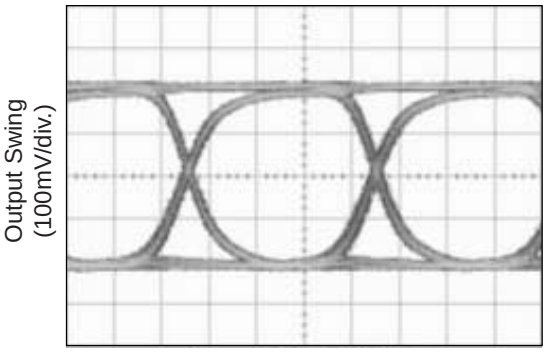

**2.5Gbps Output**



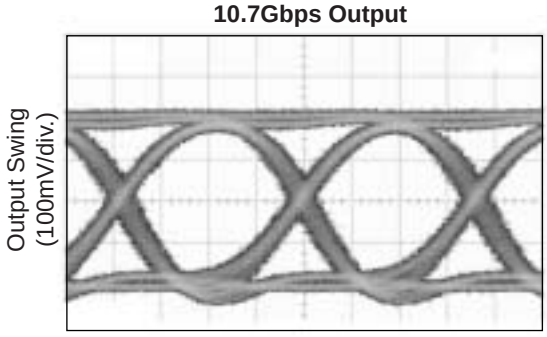

**3.2Gbps Output**




**5Gbps Output**



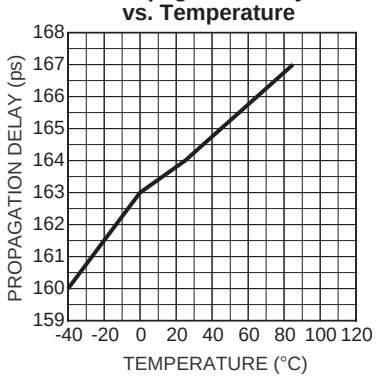

**10.7Gbps Output**



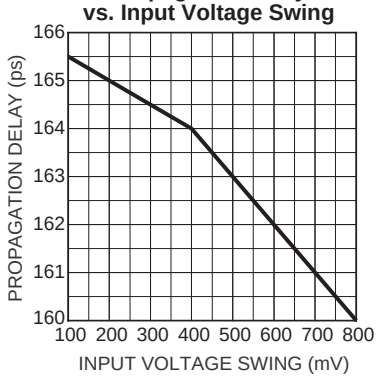
## TYPICAL OPERATING CHARACTERISTICS

$V_{CC}$ = 2.5V, $V_{IN}$ = 100mV, $T_A$ = 25°C, unless otherwise stated.

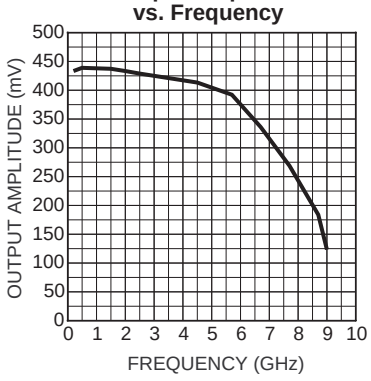
**Propagation Delay vs. Temperature**




**Propagation Delay vs. Input Voltage Swing**




**Output Amplitude vs. Frequency**



## INPUT AND OUTPUT STAGES

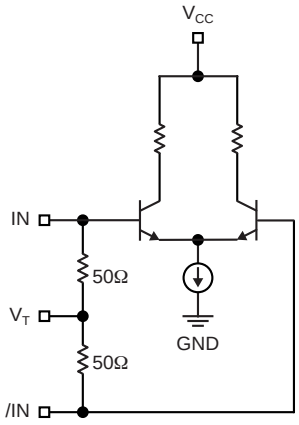



**Figure 2a. Simplified Differential Input Stage**

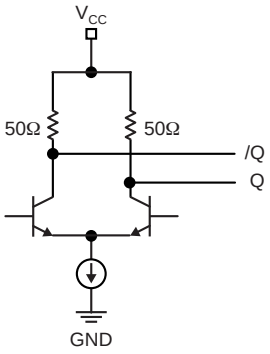



**Figure 2b. Simplified CML Output Stage**

## INPUT INTERFACE APPLICATIONS

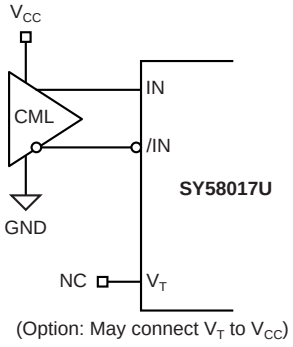



**Figure 3a. DC-Coupled CML Interface**

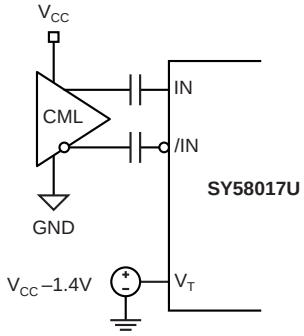



**Figure 3b. AC-Coupled CML Interface**

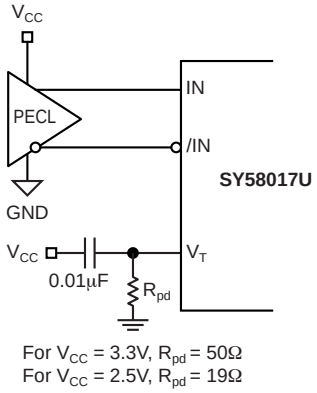



**Figure 3c. DC-Coupled PECL Interface**

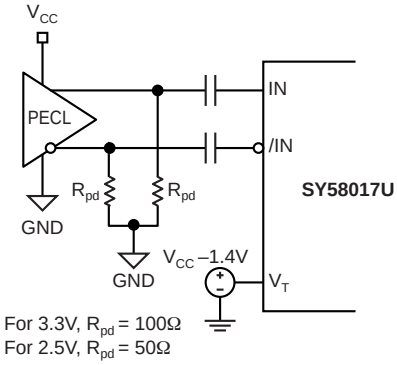



**Figure 3d. AC-Coupled PECL Interface**

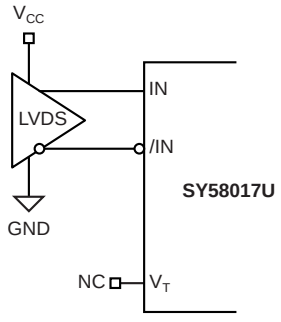



**Figure 3e. LVDS Interface**

## OUTPUT INTERFACE APPLICATIONS

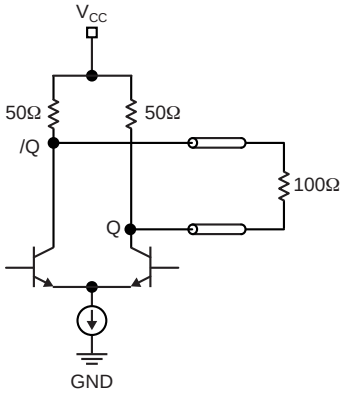



**Figure 4a. CML DC-Coupled Termination**

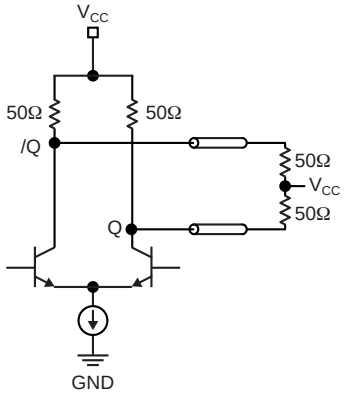



**Figure 4b. CML DC-Coupled Termination**

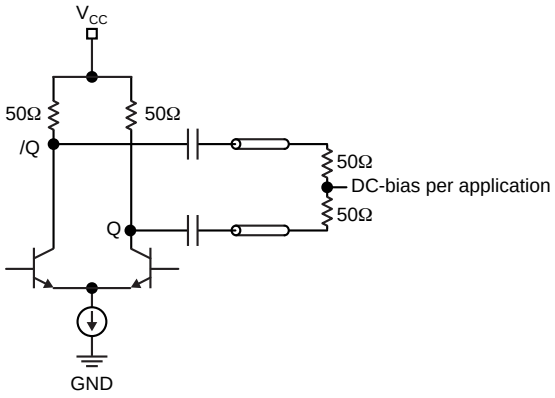
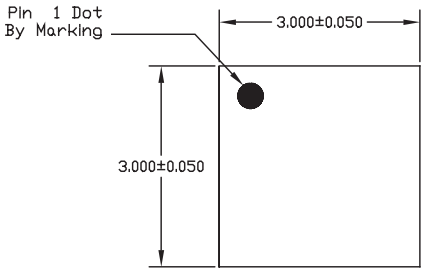



**Figure 5. CML AC-Coupled Termination**

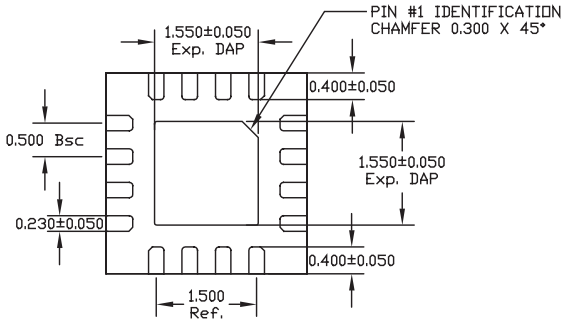
## RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

| Part Number | Function | Data Sheet Link |
|---|---|---|
| SY58016L | 3.3V 10Gbps Differential CML Line Driver/Receiver with Internal I/O Termination | http://www.micrel.com/product-info/products/sy58016l.shtml |
| SY58018U | Ultra Precision Differential LVPECL 2:1 Mux with Internal Termination | http://www.micrel.com/product-info/products/sy58018u.shtml |
| SY58019U | Ultra Precision Differential 400mV LVPECL 2:1 MUX with Internal Termination | http://www.micrel.com/product-info/products/sy58019u.shtml |
| SY58025U | 10.7Gbps Dual 2:1 CML MUX with Internal I/O Termination | http://www.micrel.com/product-info/products/sy58025u.shtml |
| SY58026U | 5Gbps Dual 2:1 MUX with Internal Termination | http://www.micrel.com/product-info/products/sy58026u.shtml |
| SY58027U | 10.7Gbps Dual 2:1 400mV LVPECL Mux with Internal Termination | http://www.micrel.com/product-info/products/sy58027u.shtml |
| SY58051U | 10.7Gbps AnyGate® with Internal Input and Output Termination | http://www.micrel.com/product-info/products/sy58051u.shtml |
| SY58052U | 10Gbps Clock/Data Retimer with 50Ω Input Termination | http://www.micrel.com/product-info/products/sy58052u.shtml |
| | MLF™ Application Note | www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf |
| HBW Solutions | New Products and Applications | www.micrel.com/product-info/products/solutions.shtml |

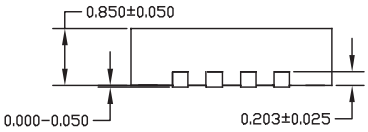
## 16-PIN *Micro*LeadFrame® (MLF-16)




TOP VIEW

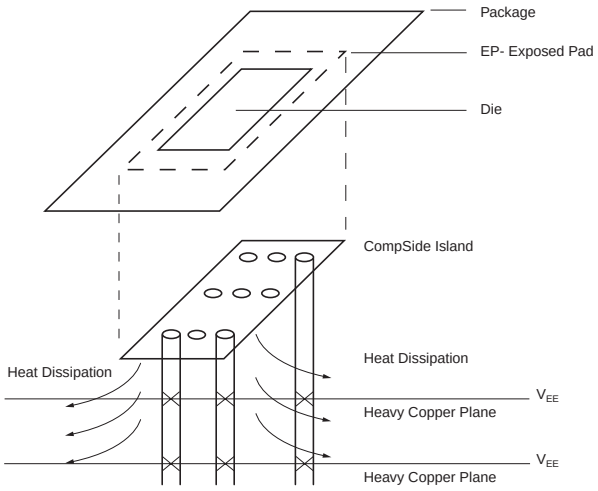



BOTTOM VIEW




SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.




**PCB Thermal Consideration for 16-Pin MLF® Package**
**(Always solder, or equivalent, the exposed pad to the PCB)**

**Package Notes:**

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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